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1 [Implementation of logical query languages for databases](#)

Jeffrey D. Ullman

September 1985 **ACM Transactions on Database Systems (TODS)**, Volume 10 Issue 3

Full text available: pdf(2.66 MB)

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We examine methods of implementing queries about relational databases in the case where these queries are expressed in first-order logic as a collection of Horn clauses. Because queries may be defined recursively, straightforward methods of query evaluation do not always work, and a variety of strategies have been proposed to handle subsets of recursive queries. We express such query evaluation techniques as "capture rules" on a graph representing clauses and predicates. One ess ...

2 [A Design Verification and Logic Validation System](#)

William A. Noon

January 1977 **Proceedings of the 14th conference on Design automation**

Full text available: pdf(679.88 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper describes an experimental design specification language which is "engineer oriented" rather than "programmer oriented." Computer programs using this language as input will Create a software model of the function description, statically and dynamically check for the completeness of the function described, check the logic implementation of the function for completeness and accuracy and generate a number of documents to provide clear communications.

3 [Noise estimation due to signal activity for capacitively coupled CMOS logic gates](#)

Kevin T. Tang, Eby G. Friedman

March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Full text available: pdf(630.94 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The effect of interconnect coupling capacitance on neighboring CMOS logic gates driving coupled interconnections strongly depends upon the signal activity. A transient analysis of two capacitively coupled CMOS logic gates is presented in this paper for different combinations of signal activity. The uncertainty of the effective load capacitance and propagation delay due to the signal activity is addressed. Analytical expressions characterizing the output voltage and propagation delay are also ...

4 [From Electron Mobility to Logical Structure: A View of Integrated Circuits](#)

Wesley A. Clark

September 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 3

Full text available: pdf(3.29 MB)

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